

1 1 1 1

1 0 1 0

X X X X

1 1 X X

g = A + BC’ + CD’ +B’C

0 0 1 1

1 1 0 1

X X X X

1 1 X X

f = A + C’D’ + BC’ + BD’

1 0 0 0

1 1 0 1

X X X X

1 1 X X

e = B’D’ + CD’

1 0 0 1

0 0 0 1

X X X X

1 0 X X

c = C’ + B + D

1 1 1 0

1 1 1 1

X X X X

1 1 X X

a = C’ + A + BD + B’D’

1 0 1 1

0 1 1 1

X X X X

1 1 X X



**OPTIMIZATION**

d = A + B’C + B’D’ + BC’D + CD’

1 0 1 1

0 1 0 1

X X X X

1 1 X X

b = B + C’D’ + CD

**Verilog Code**

module ODEV(input [3:0] bcd, output reg [6:0] sevenseg);

always @(\*)

case (bcd)

4'b0000:sevenseg = 7'b1111110;

4'b0001:sevenseg = 7'b0110000;

4'b0010:sevenseg = 7'b1101101;

4'b0011:sevenseg = 7'b1111001;

4'b0100:sevenseg = 7'b0110011;

4'b0101:sevenseg = 7'b1011011;

4'b0110:sevenseg = 7'b1011111;

4'b0111:sevenseg = 7'b1110000;

4'b1000:sevenseg = 7'b1111111;

4'b1001:sevenseg = 7'b1111011;

default :sevenseg = 7'b0110110;

endcase

endmodule

### Applications of Display Decoder Circuit

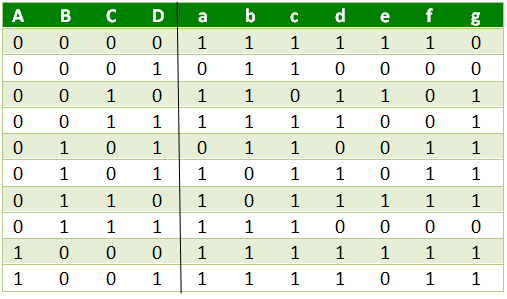
1. This circuit can be modified using timers and counters to display the number of clock pulses.
2. This circuit can be modified to develop an alphabet display system instead of a decimal number display system.
3. It can be used as a timer circuit.

**Introduction**

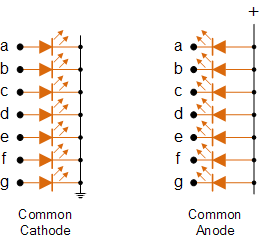
Usually seven-segment displays are used to display the digits in digital watches, calculators, clocks, measuring instruments and digital counters, etc. Generally, LCD and LED segments provide the display output of numerical numbers and characters. However to display the characters and numbers, seven-segment displays are most commonly used.

A display decoder is used to convert a BCD or a binary code into a 7 segment code. It generally has 4 input lines and 7 output lines. Using Karnough’s map, logic circuitry for each input to the display is designed.

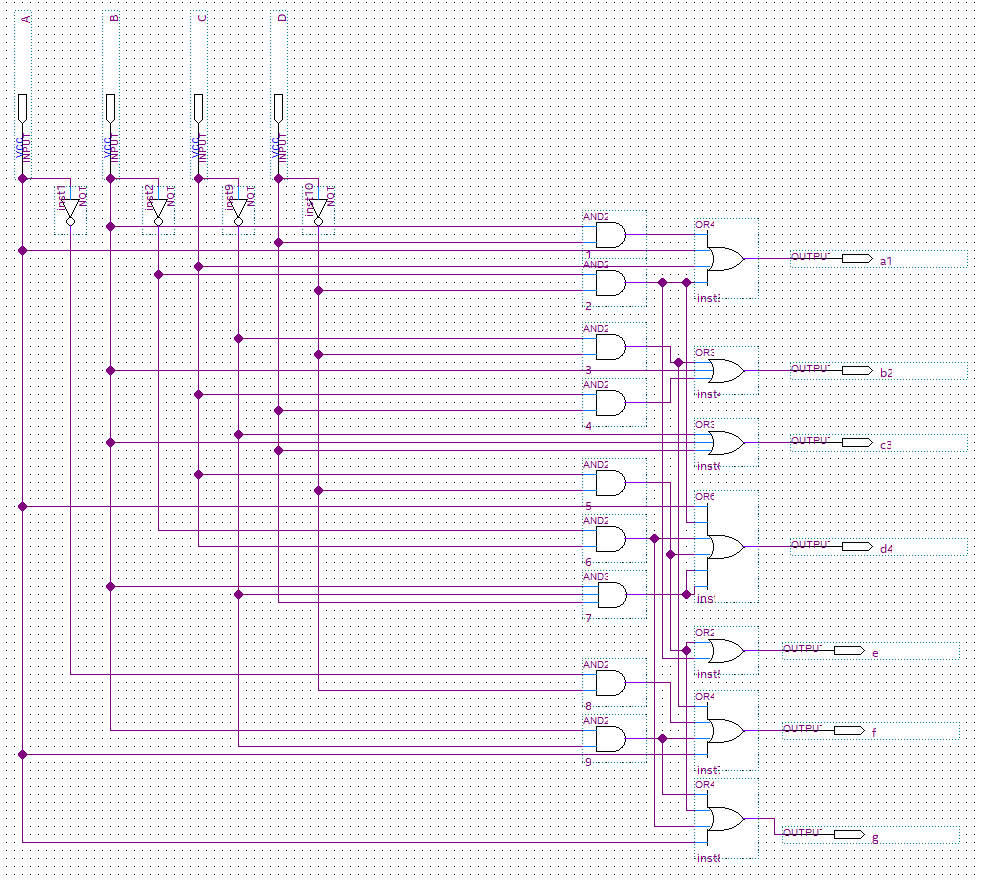
**Table Of Truth**

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First of all, the truth table is made. There is don’t care states below the nine. Don’t cares doesn’t change the result. We can use don’t cares as 1 or 0.



The screens were considered as common anodes. In this way, you just need to give 1.

**Gate Realization and Cad Simulation**

